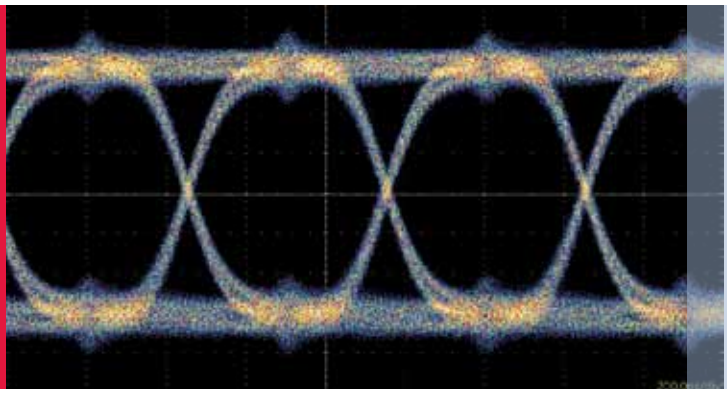

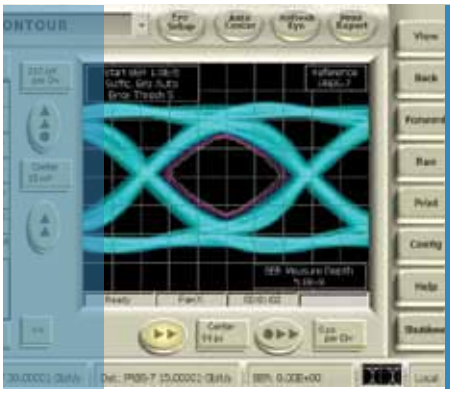

# Physical Layer Tests of 100 Gb/s Communications Systems

Application Note

Tektronix®

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# 1. Introduction

The list of bandwidth intensive applications has exploded in the last decade. Video-on-demand, voice-over-IP, cloud-based computing and storage have created a ravenous bandwidth appetite that is rushing deployment of 100 Gb/s technology.

The power of High Speed Serial (HSS) technology, with its noise resistant differential signaling and jitter resistant embedded clocking plus closed-eye equalization, enables 25+ Gb/s on previously inconceivable lengths of Printed Circuit Board (PCB). Combining HSS links in parallel simplifies 100G signal transmission to optical transceivers, easing connectivity to the fiber optic backbone. The result is that many datacom and telecom technologies are using 100 Gigabit Ethernet (100 GbE) for transport, including SAS, Infiniband, even Fibre Channel – it's even replacing venerable SONET/SDH.

The rush to deploy 100G technology without a great deal of industry experience at 25+ Gb/s rates makes it more important than ever to understand how analog waveforms relate to digital signal Bit Error Rates (BER). Consider this: the bit period at 25 Gb/s is 40 ps. The jitter budget has all but disappeared. Less than 3 ps of random jitter closes the eye altogether; emerging standards typically permit less than 700 fs of RJ.

This note covers the transmitter and receiver tests necessary to assemble a 100G system. Since every 25+ Gb/s HSS technology shares common themes, we'll follow 100 GbE compliance requirements but point out differences between the other high rate systems like Fibre Channel's 32GFC. Where the 100 GbE specification has gaps – like in 25-28 Gb/s electrical signaling – we'll employ the Implementation Agreements of the Optical Internetworking Forum's Common Electrical Interface (OIF-CEI).

As we work through the tests we'll encounter common themes in the interplay of jitter, noise, and crosstalk. Following the description of compliance tests, we'll suggest tests that can help diagnose noncompliant components and systems as well as measure performance margins.

| Standard | | Geometry | Reach | Data rate | BER |
|---|---|---|---|---|---|
| 100 GbE | 100GBASE-LR4<br>100GBASE-ER4 | 4 SM fibers | 10 km 40 km | 4x25.78125 Gb/s | ≤ $10^{-12}$ |
| | 100GBASE-SR4* | 4 MM fibers | ≤ 10 m | 4x25.78125 Gb/s | ≤ $10^{-12}$ |
| | 100GBASE-CR4*<br>100GBASE-KR4* | 4 cables, backplane | * | * | ≤ $10^{-12}$ |
| OIF-CEI | OIF-28G-SR<br>OIF-28G-VSR* | *N* traces on PCB | 30 cm 15* cm | 19.90-28.05 Gb/s | ≤ $10^{-15}$ |
| Fibre Channel | 32GFC | *N* channels optical and electrical | TBA* | 28.05* Gb/s | ≤ $10^{-12}$* |

**Table 1.** Summary of emerging standards (standards marked with an asterisk, *, have not been released, consider the values speculative).

# 2. Emerging 100 Gb/s and related standards

Standards recommend tests to assure component interoperability. In this section, we summarize the specifications, Table 1. It's important to keep in mind that since most of the standards have not been published, the numbers we quote should be considered typical of what to expect, but for compliance testing, check the actual standards for specific numbers!

Technology specifications tend to be written in the engineering equivalent of legalese, so we composed this note as a supplement to clarify the tests themselves, their role, and how to perform them.

At the electrical end, the technology shares these characteristics: balanced, unidirectional, 100 Ohm, differential signaling with embedded clocks, low voltage swings, Non-Return to Zero (NRZ) signals, and multiple channels.

Since terminology varies among the specifications, let's clear up potential misunderstandings immediately. In this document, we distinguish the data rate and payload rate; the data rate is the rate at which raw data propagates. The payload rate does not include overhead from error correction and coding, hence, payload rate ≤ data rate. Since we'll only discuss NRZ signaling, we use Gb/s rather than Gbaud and equate the terms "symbol" and "bit."

## 2.1. 100 GbE – IEEE Std 802.3ba

We'll draw from two established 100 GbE optical transmission specifications, Table 1, both covered in the IEEE Std 802.3ba standard, Long Reach, **100GBASE-LR4**, and Extended Reach, **100GBASE-ER4**. The differences between them are primarily at the receive end. The ER4 receiver has greater sensitivity and has to pass a more difficult stress tolerance test than the LR4 receiver.

As this Application Note is written, the Short Reach, 100GBASE-SR4, 4×25 Gb/s low cost, Multi-Mode (MM) standard, along with those for electrical transport over cables and backplanes, 100GBASE-CR4 and 100GBASE-KR4, are works in progress. When finished, the 100GBASE specifications will provide a complete suite of optical interconnect systems.

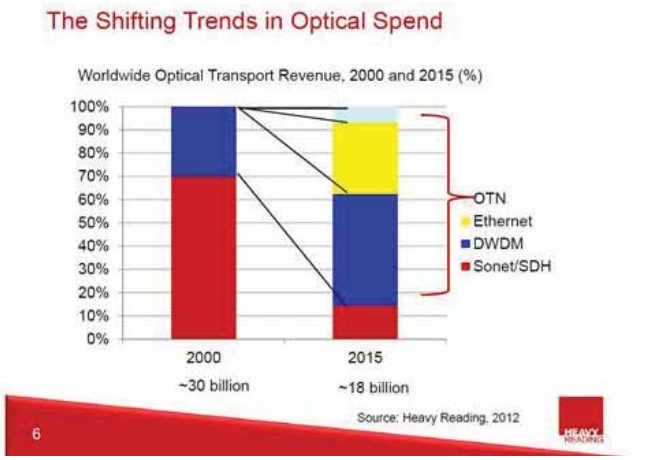


**Figure 1.** Comparison of optical transport revenue from 2000 and 2015 (graphic Copyright 2012, Heavy Reading).

### SONET/SDH

In the last decade, Ethernet has emerged as the default choice for all networking, both datacom and telecom. The chart in Figure 1 predicts that by 2015 ONET/SDH will drop in optical transport revenue from 70% to less than 15%.

## 2.2. 100 OIF CEI

Implementation Agreements (IAs) from the OIF-CEI do not prescribe compliance tests the way that IEEE's 802.3ba 100 GbE, or FiberChannel specifications do. Instead, the emphasis is on informative and normative tests that attempt to assure component interoperability across standards. "Normative" tests are like compliance tests in the sense that the committee prescribes them to assure interoperability whereas "informative" tests are recommended to develop a more thorough understanding of performance and margin.

In this note, we draw from the two OIF-CEI IA's summarized in Table 1.

The short reach IA, **OIF-28G-SR** consists of multiple lanes at 19.90-28.05 Gb/s of differential pairs over 300 mm of PCB with up to one connection operating at BER < $10^{-15}$.

The very short reach IA, **OIF-28G-VSR** has not been published, but we take guidance from the preliminary version. It consists of multiple electrical lanes at 19.60-28.05 Gb/s for signaling between Serdes (called hosts in the IA) and transceivers (modules in the IA). The Serdes and transceiver can be separated by some 100 mm of PCB to a connector, plus an additional 50 mm or so of conducting trace; the system is required to operate at BER < $10^{-15}$.

## 2.3. Fibre Channel 32GFC

The high rate Fibre Channel standard, 32GFC, has a data rate of 28.05 Gb/s. The confusing name scheme, 32GFC for 28.05 Gb/s technology, comes from the desire for the name of each generation to demonstrate that the payload rate, as opposed to the data rate, is double that of the previous generation. The confusion began with a large decrease in overhead in the transition from 8GFC to 16GFC when the data rate advanced from 8.5 to 14.025 Gb/s but the payload rate doubled from 6.4 to 12.8 Gb/s. The payload rate for 32GFC is 25.6 Gb/s, twice that of 16GFC, but the data rate, 28.05 Gb/s, is well short of that implied by the 32GFC abbreviation.

As this note is written, the 32GFC has not been published and the preliminary version has few reference values.

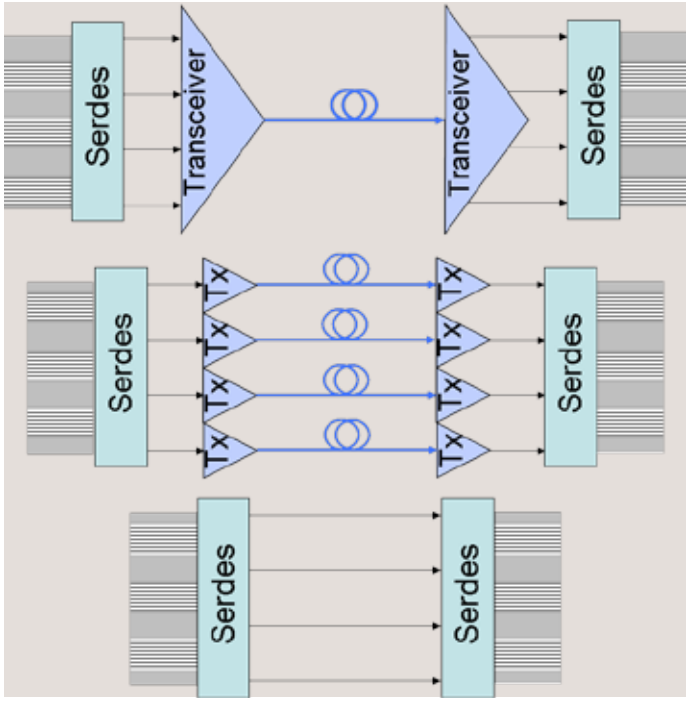


**Figure 2.** Diagram of (a) 4×25 Gb/s 100G Serdes-Transceiver WDM optical system, (b) 4×25 Gb/s 100G Serdes-Transceiver optical system, and (c) a 4×25 Gb/s 100G Serdes to Serdes electrical system. The figure does not show the symmetric return paths.

## 3. Testing 100G Systems

Figure 2 is a diagram of the components of typical 100G systems. A Serdes serializes a signal and transmits four 25+ Gb/s differential pairs. The Serdes may be integrated or might consist of separate components for each output. The 25+ Gb/s electrical signals are transmitted from the Serdes to an optical transceiver. The transceiver retimes the signals and transmits optical versions on either Single Mode (SM) or Multi-Mode (MM) optic fibers. A second transceiver receives the optical signals, converts them to electrical and transmits them to another Serdes for deserializing. The purely electrical version follows the same scheme without the intermediate transceiver-driven optical signaling.

| Test patterns | |
|---|---|
| 0x00ff square wave | 8 bits low, 8 bits high |
| PRBS9 | 511 bits |
| PRBS15 | 32,767 bits |
| PRBS31 | 2.1 Gbits |
| Scrambled idle | |
| OIF CID jitter tolerance pattern | (72 CID bits + ≥ 10328 from PRBS31 + seed) + complement |

**Table 2.** Test Patterns.

Whether for transmitter or receiver testing, optical or electrical, we need test patterns that put every aspect of a component and every component of a system to the test. The Pseudo Random Binary Sequences (PRBS*n*) are standardized patterns with every permutation of n bits. The OIF CID jitter tolerance pattern is designed to have the most aggressive elements of the PRBS31, plus 72 bit sequences of Consecutive Identical (CID) bits but at a manageable length.

The Tektronix BERTScope Bit Error Ratio Tester provides all test patterns used in 100G communications, including PRBS31, scrambled idle, or for that matter, every common test pattern as well as any that you devise, up to 128 Mb in length.

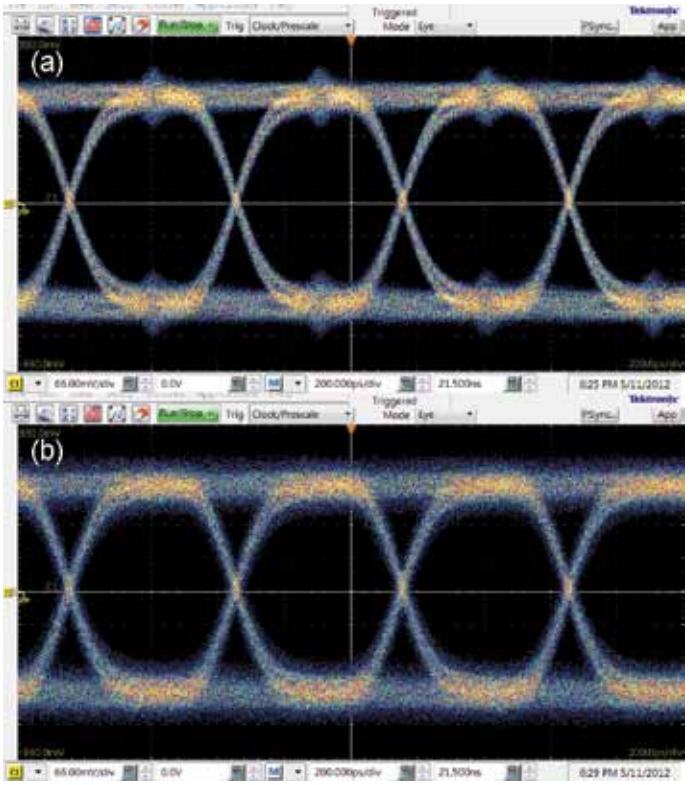


**Figure 3.** Victim eye diagrams for (a) synchronous and (b) asynchronous crosstalk.

All transmitter tests, both electrical and optical, should be performed with every system channels active in both directions to include all reasonable sources of crosstalk interference. To prevent unrealistic data-dependent interference, test patterns on the crosstalk channels should differ from the test signal pattern. If it's not possible for each aggressor to transmit a unique pattern, at least introduce sufficient delay between them so that the patterns aren't synchronized.

Crosstalk channels should also operate with asynchronous timing for a couple of reasons: first, except in special cases, each channel operates with a clock that has been independently recovered from its incoming data. While each clock operates at the same nominal rate, they are neither frequency locked nor phase locked, which is to say, they're not in synch. Second, as shown in Figure 3, synchronous crosstalk has different properties than asynchronous crosstalk. Synchronous crosstalk degradation occurs in the same region of the test signal eye diagram every time an aggressor makes a logic transition. Asynchronous crosstalk, on the other hand, causes randomly timed degradation.

If your Serdes is integrated on a single chip with multiple serialized outputs you have to watch out for inter-chip crosstalk. If the outputs are timed with a common clock, then they should be active, synchronized with the test channel, and each channel should transmit a unique signal.

Since the frequency response of PCB punishes high frequency content, electrical signaling between Serdes chips or between Serdes and transceivers across centimeters of PCB requires signal conditioning: pre-emphasis at the transmitter and equalization at the receiver.

Stressed receiver tolerance tests are designed to assure that every compliant receiver can operate at the specified BER even with the worst-case compliant input signal. For 100 GbE IEEE 802.3ba and Fibre Channel 32GFC the specified BER is $10^{-12}$, for OIF-CEI it is $10^{-15}$.

| Summary of 100 GbE optical transmitter recommendations | | |
|---|---|---|
| | 100GBASE-LR4 | 100GBASE-ER4 |
| Average launch power | -4.3 to 4.5 dBm | -2.9 to 2.9 dBm |
| Optical modulation amplitude | -1.3 to 4.5 dBm | 0.1 to 4.5 dBm |
| Extinction ratio | 4 dB | 8 dB |

**Table 3.** Summary of transmitter recommendations.

## 3.1. Testing optical transmitters

Transmitter recommendations are summarized in Table 3.

Optical eye diagrams for 100GBASE-SR4 and 100GBASE-ER4 4×25 Gb/s geometries of 100 GbE are shown in Figures 4a and 4b. The normalized logic 0 and 1 levels used in the eye-mask are defined by the averages of the lower and upper halves of the central 0.2 UI of the eye.

**Eye mask** tests can be performed on either a DSA8300 low noise equivalent time sampling oscilloscope or a BERTScope. In both cases, wide bandwidth optical-to-electrical receivers and clock recovery units are necessary. The clock recovery -3 dB bandwidth differs among specifications, typically $f_{data}$/1667, and can be accommodated by CR286A, a full, digital-based, second order Phase-Locked Loop (PLL) with user-specified corner frequencies capable of tracking jitter to 24 MHz.

The optical-to-electrical receiver should apply a 4th order Bessel-Thompson filter with a reference frequency of three-fourths the data rate, ¾ $f_{data}$. The filter is not included to provide the appropriate response of a compliant optical receiver, rather, it's required so that different test platforms can operate under uniform measurement conditions.

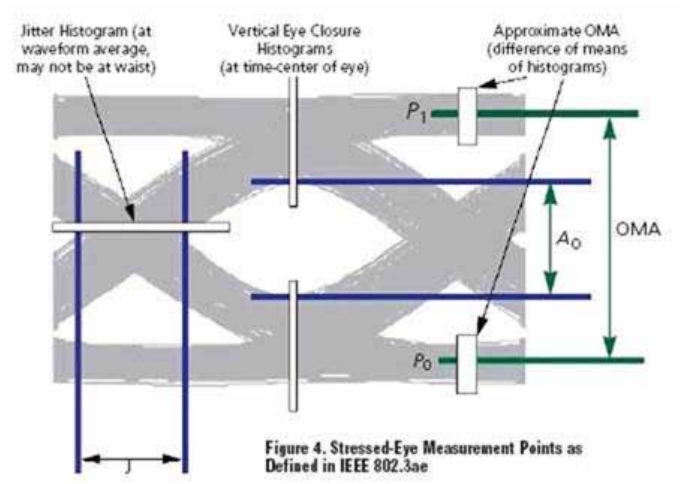


**Figure 4a.** Effect of low pass Bessel-Thompson filter on stressed eye calibration. Rolls off frequency content in excess of 20 GHz. Image courtesy of IEEE802.3ba standard.

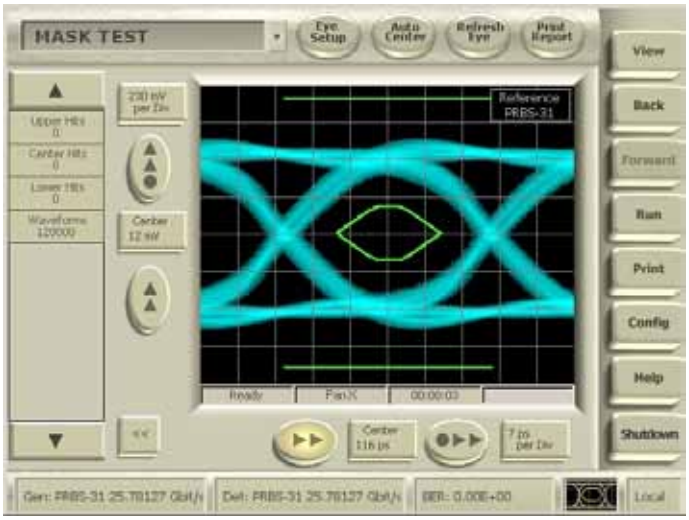


**Figure 4b.** 100GbE Eye Mask on a BERTScope.

The random nature of a mask test is addressed by requiring a minimum "hit ratio." The hit ratio is defined as the ratio of the number of mask violations to the total number of samples acquired per unit interval. Since this is a statistical measurement, it's worthwhile to keep in mind that the more hits the greater the accuracy.

A transmitter is compliant if it achieves a hit ratio less than $5\times10^{-5}$.

Alternatively, it's both more statistically reliable and easier to measure the BER Contour on a BERTScope or on a DSA8300 equipped with 80SJNB jitter and noise analysis software. As long as the BER=$10^{-6}$ contour is outside the mask, Figure 5a, the transmitter passes the $5\times10^{-5}$ hit ratio eye test. The BER Contour technique also makes it easier to see the margin with which a transmitter passes. As shown in Figure 5b, the BERTScope is using BER Contour to evaluate J9 performance on a signal with additional margin performance (30 Gb/sec).

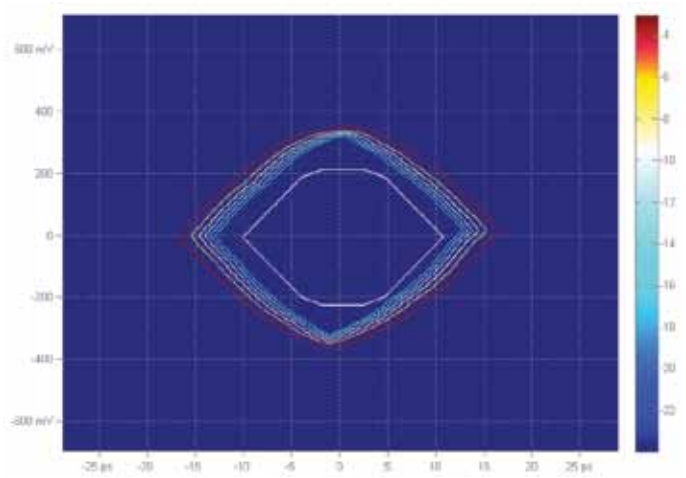

**Figure 5a.** Eye mask testing with BER contours. The BER=$10^{-6}$ contour, the outer yellow-orange contour, corresponds to a $5\times10^{-5}$ hit ratio.

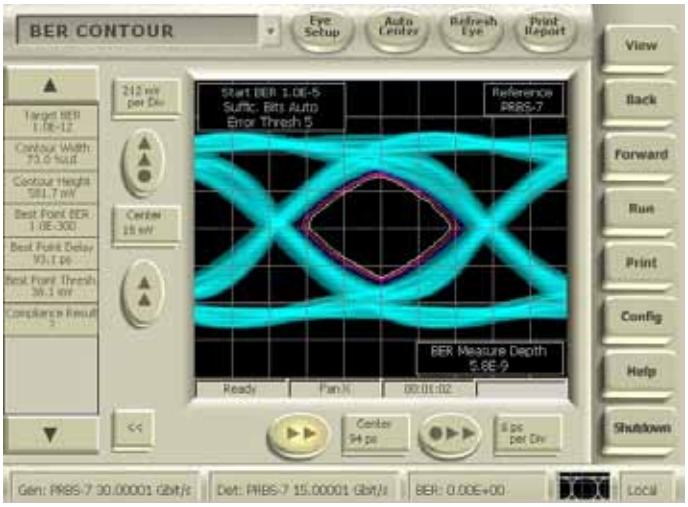


**Figure 5b.** BER Contour for J9 with BERTScope using a 30 Gb/sec signal.

| Typical 100GbE Stressed Optical Receiver Tolerance Test Conditions | | | |
|---|---|---|---|
| | 100GBASE-LR4 | 100GBASE-ER4 | Frequency |
| Average received power | 4.5 to -10.6 dBm | 4.5 to -20.9 dBm | |
| Sinusoidal Jitter (SJ) | 0.05 above roll off frequency, see Figure 5 | | |
| Sinusoidal interference | Sum to J2 and J9 | | 0.1-2 GHz |
| RJ | | | |
| J2 jitter | 0.3 UI | | |
| J9 jitter | 0.47 UI | | |

**Table 4.** Summary of 100 GbE stressed receiver sensitivity test conditions. The sum of effects from all stressors is prescribed to meet the vertical eye closure and J2 and J9 jitter specifications.

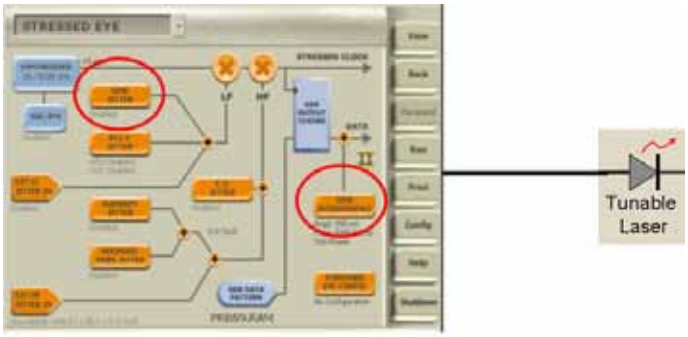


**Figure 6.** Sinusoidal Interferers directly from the BERTScope driving a laser for Optical Receiver Testing.

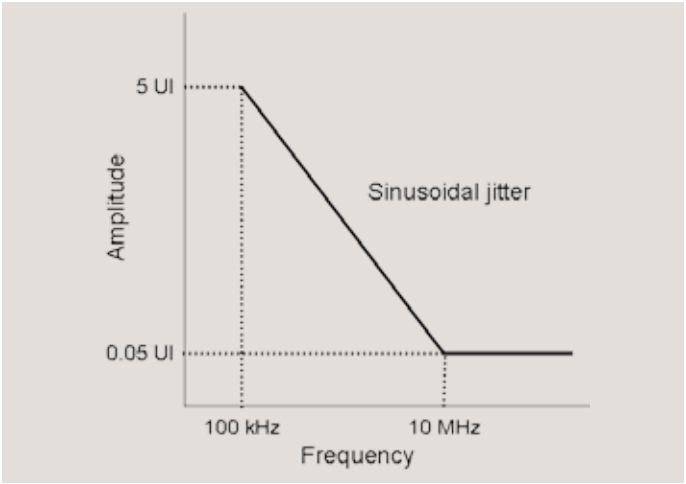


**Figure 7.** Sinusoidal Jitter stress template.

## 3.2. Testing optical receivers

The optical receiver stress tests for the long and extended reach 4×25 Gb/s topologies (100GBASE-LR4 and 100GBASE-ER4) are similar except that greater sensitivity and robustness is required of ER4, as indicated in Table 4,

Figure 6 shows how to apply calibrated levels of stress to the test signal and Table 4 summarizes the stresses. At these data rates, producing compliant stress levels is tricky. With option STR, the BERTScope can generate a conformant, stressed eye using its internal impairment system for driving a tunable laser-based signal into the optical receiver device under test. (see Figure 6)

First, configure the BERTScope to drive a Mach-Zehnder (MZ) optical modulator. Then tune the MZ bias to optimize 1/0 symmetry, but don't exceed the Optical Modulation Amplitude (OMA) given in Table 4.

Apply Sinusoidal Jitter (SJ) to the pattern generator clock according to the template in Figure 7 to assure that the receiver can track low-frequency jitter.

Generate Inter-Symbol Interference (ISI) with a 4th order Bessel-Thompson filter. As specified by the IEEE802.3ba Stress-Conditioning Block, this 19 GHz low-pass filter characteristic removes higher order harmonics from the test generator output to permit a more consistent approach to measuring the vertical eye closure penalty and data-dependent jitter (DDJ).

Apply Random Jitter (RJ) with a precision Gaussian noise generator. Gaussian RJ can be imposed on a signal by adding the noise and then subjecting the signal to a limiting amplifier. For the precision required at these data rates, the AM-to-PM conversion of a limiter is an ideal method for applying RJ.

Though not yet required in a standard that has been released, expect to see **Random Noise (RN)** required in specifications as we get more experience at 25+ Gb/s. RN will also be introduced by adding precision Gaussian noise to the signal but without a limiter, of course.

Setting **Vertical Eye Closure Penalty (VECP)** to the level given in Table 4 is a multi-step process. Optical VEC is given by:

$$\mathrm{VECP} = 10\log\frac{OMA}{\mathrm{EH}(2.5\times10^{-3})}$$

where the eye height, EH($2.5\times10^{-3}$), is the vertical eye opening defined at a BER. While conceptually cumbersome, EH(BER) is a more precise definition than average peak-to-peak voltage swing. It is equivalent to the vertical distance at the center of the eye between BER contours of $2.5\times10^{-3}$ which is easy to measure on either the BERTScope or DSA8300 with 80SJNB software.

Tune the **J2 and J9 jitter** levels after setting VECP. J2 and J9 indicate the properties of the jitter distribution. The high probability jitter, 99% of the distribution, is contained in J2, hence J2 is equivalent to the Total Jitter (TJ) defined at BER = $2.5\times10^{-3}$. On the other hand, J9 indicates the low probability, RJ dominated tails of the jitter distribution, the outer billionth; hence J9 is equivalent to TJ at BER = $2.5\times10^{-10}$.

Add sinusoidal interference (amplitude modulation) to the signal, until the J2 requirement is reached, Figure 8.

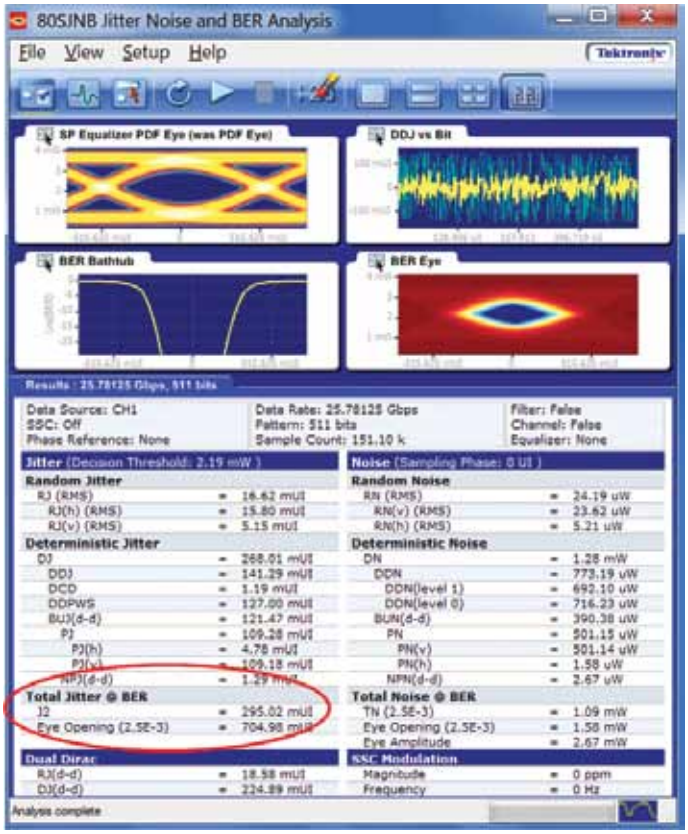


**Figure 8.** Example measurement of J2 on the DSA 8300 with 80SJNB.

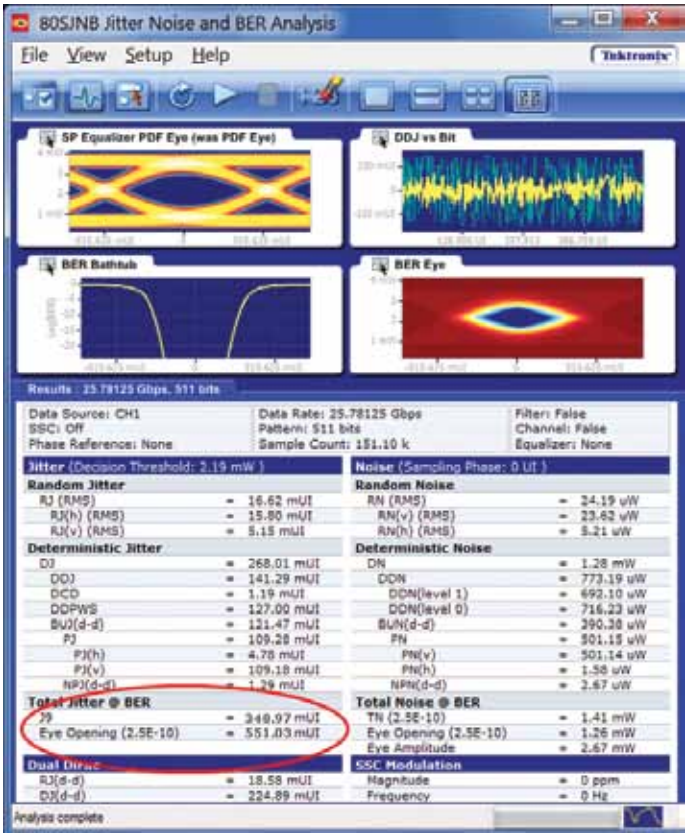


**Figure 9.** After setting J2, the J9 level is 0.35 UI, to meet the J9 spec, add less than 335 fs rms RJ.

Because of the wide BER disparity between J2 and J9, a tiny amount of rms RJ raises J9 to the required level with only a tiny effect on J2. For example, Figure 9, if after setting J2, the J9 level is 0.35 UI, to meet the 0.47 UI J9 spec, add 0.12 UI of RJ – **that's less than 335 fs of rms RJ**. Particular care needs to be taken to ensure the intrinsic Rj of the generator source is lower than 332 fs, otherwise a simultaneous J2 and J9 intercept as shown in Figure 9 becomes impossible. To add very small amounts of Rj beyond the noise floor of the instrumentation we use a precision rj noise source to add femtosecond levels of RJ into the signal path. Very little incremental Rj typically needs to be added to intercept the J9 jitter level. It's vitally important in this step that the BERTScope generator and DSA8300 sampling scope are used together in the calibration work as a system.

Transmit the stressed signal into a replication of the system, Figure 11, along with three other signals for crosstalk.

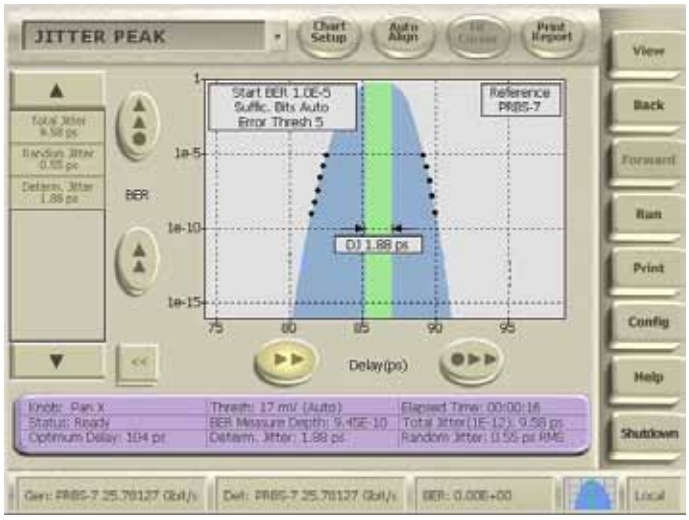


**Figure 10.** Jitter Peak with J9 measured on a BERTScope.

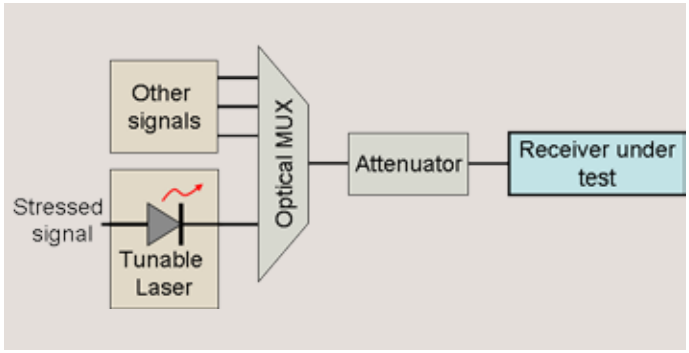


**Figure 11.** Optical stressed receiver test.

If the receiver is capable of counting its own BER, testing can be completed. If not, connect the receiver output to the BERTScope. If the receiver doesn't provide a clock output, you should use a clock recovery unit to time the error detector. If you don't have a clock recovery unit, you might be able to use the BERTScope clock output since the output of the receiver has been retimed and should be pristine.

Apply the stressed signal to the receiver, first with low amplitude SJ applied above the roll off frequency in the template of Figure 7. If the receiver operates at BER $\leq 10^{-12}$, then with all other stresses applied, continue the tests across the SJ frequency-amplitude template in Figure 7. It's automatic with the BERTScope's Jitter Transfer Measurement function.

If the receiver operates at BER $\leq 10^{-12}$ for all tests, it's compliant.

| Typical electrical transmitter requirements | |
|---|---|
| Data rate (c.f., baud rate) | 19.90-28.05 Gb/s |
| Equivalent reach on standard FR-4 PCB with one connector | 10-30 cm |
| Compliance test board insertion loss at Nyquist frequency | -1.75 to -1.25 dB |
| Pre-emphasis<br>Pulse response optimization | ≥ 3 taps<br>≥ 8 UI |
| Peak-to-peak differential voltage | 800-1200 mV |
| Rise/fall time (20/80%) | ≥ 8-10 ps |
| Vertical Eye Closure (VEC) | ≤ 3-9 dB |
| Duty-Cycle-Distortion (DCD) | ≤ 0.035 UI |
| Uncorrelated Deterministic Jitter (e.g., SJ + DCD) | ≤ 0.15 UI |
| Random Jitter (RJ at BER=$10^{-15}$) | ≤ 0.15 UI |
| Eye width at BER = $10^{-15}$, EW<br>Total Jitter at BER = $10^{-15}$, TJ | ≥ 0.46-0.72 UI<br>≤ 0.28-0.54 UI |
| Eye height at BER = $10^{-15}$, EH | ≥ 100-300 mV |

**Table 5.** Summary of typical electrical transmitter requirements.

## 3.3. Testing electrical transmitters

Typical electrical transmitter requirements are given in Table 5.

The broad range of requirements in Table 5 demonstrates the differences in the three separate electrical signaling subsystems shown in Figure 2: Serdes→Serdes, Serdes→transceiver, transceiver→Serdes. The Serdes→Serdes geometry at the bottom of Figure 2 has the longest reach and most stringent requirements. The Serdes→transceiver case has the most relaxed requirements, and transceiver→Serdes is intermediate.

Transmitter characteristics can be measured on either an DSA8300 or BERTScope. In either case, a reference receiver is required with a golden PLL, such as the clock recovery unit CR286A.

The transmitted signal amplitude specification is given in terms of Eye Height defined with respect to BER, EH(BER). Eye Width is also defined in terms of BER, EW(BER); it might be more familiar because it's related to TJ which is also defined with respect to BER. Where TJ is eye closure, EW is eye opening.

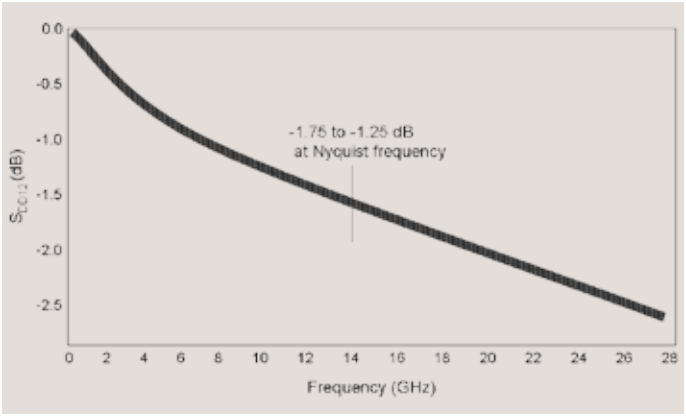


**Figure 12.** Differential frequency response of typical compliance test boards.

Since electrical transmitters at these rates apply signal pre-emphasis to partially correct channel response, rather than testing transmitted signals right out of the spigot, compliance test boards are inserted between the transmitter outputs and test equipment. Typical Nyquist rate ($f_{data}/2$) loss values for compliance boards are given in Table 5 and Figure 12 shows a typical differential response.

Just as each specification has different requirements motivated by application and length of transmission on PCB, they also require compliance boards with different loss and frequency response profiles. Tektronix can provide a variety of calibrated trace lengths. In some cases the role of compliance test boards can also be automated.

At least **three taps of pre-emphasis** are required. Three taps means that the voltage levels of a bit making a transition as well as those preceding and following it are modified to compensate for the channel frequency response. The tap values, $C_{-1}$, $C_0$, $C_1$, are derived from at least 8 UI of the channel pulse response. Think of the ISI introduced by the channel as the effect of folding the channel frequency response over the profile of each transmitted bit. The resulting waveform of each bit can extend over many UI. Typical 25+ Gb/s specifications require optimization over at least 8 UI.

It's reasonable to test the transmitter with intermediate, run-of-the-mill pre-emphasis values. Introduce the compliance board, choose a trace that's about the minimum prescribed length, and optimize the transmitter pre-emphasis scheme. If the resulting pre-emphasis level is less than half that allowed, use a slightly longer trace. If it's much larger than half that allowed, try a slightly shorter trace.

Remember, eye diagrams at these data rates, even after transmission across just a few cm of PCB, can be closed at the receiver even with pre-emphasis. So some specifications also require that the test equipment apply a Continuous Time Linear Equalization (CTLE) scheme. This way the interaction of transmitter pre-emphasis and minimal receiver equalization is included in the test. The CTLE is typically a single zero, two-pole filter that peaks at the Nyquist rate, $f_{data}/2$.

Different specifications require different test patterns. For transmitter testing, a PRBS9 pattern is usually sufficient. Of course, all other system channels should be active so that crosstalk is included in the tests. Crosstalk aggressors should transmit different patterns and, to the extent possible, for the reasons discussed above, the aggressors should be asynchronous.

You can perform the tests with either a DSA8300 or BERTScope triggered with a clock recovered from the signal. The appropriate clock recovery module for these data rates is CR286A, check the specifications to make sure you apply the correct 3 dB bandwidth, usually $f_{data}/1667$.

**Eye Height and Eye Width** defined with respect to BER, EH(BER) and EW(BER), are easy to measure with a BER-eye diagram on the DSA8300 equipped with 80SJNB BER analysis software (see Figure 13) or a BER Contour on the BERTScope.

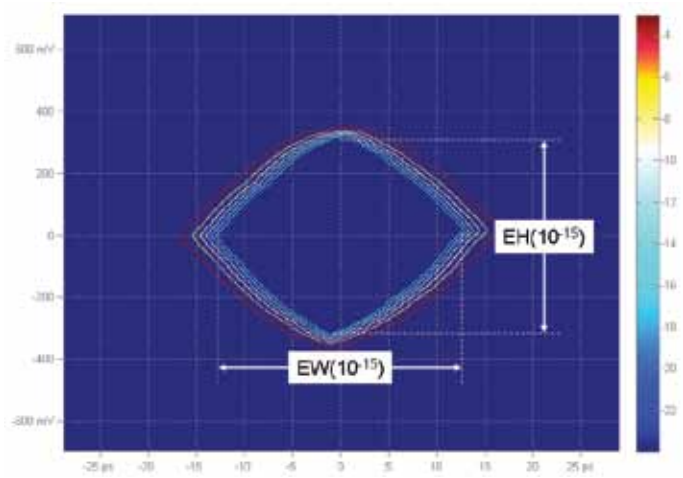


**Figure 13.** Measurements of EH($10^{-15}$) and EW($10^{-15}$) with a BER Eye diagram.

With the compliance board in place and pre-emphasis optimized. Configure the CTLE gain as defined by the spec, typically 1 to 3 dB, to produce the greatest EH(BER). If you're using the DSA8300, collect at least 12 million samples; if you're using a BERTScope acquire at least 4 million bits. The greater the statistical sample, the better.

EH($10^{-15}$) is the vertical separation of the inner BER=$10^{-15}$ contours at the center of the eye. Similarly, EW($10^{-15}$) is the horizontal separation of the inner BER=$10^{-15}$ contours at the eye center.

Vertical Eye Closure (VEC) is the ratio of the average voltage swing and eye height:

$$\mathrm{VEC} = 20\log\frac{V_{avg\,swing}}{\mathrm{EH}(10^{-15})}$$

On the BERTScope, you can read the average voltage swing right off the BER contour. On the DSA8300, you have to acquire an eye diagram with at least 12 million samples, as before, to get reliable average high and low logic levels. Their difference is the average voltage swing.

| Serdes and transceiver stressed eye receiver test summary | |
|---|---|
| Test Pattern | PRBS31 |
| Compliance test board insertion loss at Nyquist frequency | -2.5 to -1.5 dB |
| SJ at frequency above roll off in Figure 7 | 0.05 UI |
| DJ via low pass filter + BUJ-crosstalk + RJ to get TJ(10-15) = | 0.28 UI |
| Swing voltage | 600 mV |
| Sinusoidal interference so that EH($10^{-15}$) = and TJ($10^{-15}$) = | 240 mV<br>0.43 UI |
| BER for any SJ amplitude and frequency in Figure 7 | ≤ $10^{-15}$ |

**Table 6.** Summary of Serdes and transceiver electrical stressed eye specifications.

## 3.4. Testing electrical receivers

Stressed receiver tolerance testing is meant to subject the receiver to the worst case signal. If the receiver, including its internal equalization scheme, operates at or less than the prescribed BER, BER ≤ $10^{-12}$ for 100 GbE and 32GFC, and BER ≤ $10^{-15}$ for OIF-CEI, then the receiver is compliant.

Each specification requires different levels and types of stress. Some only require SJ. In this section, we include representative stresses from the standards described in Section 2, with typical levels quoted in Table 6. Be sure to check the specification to which you are testing to guarantee that your test is compliant.

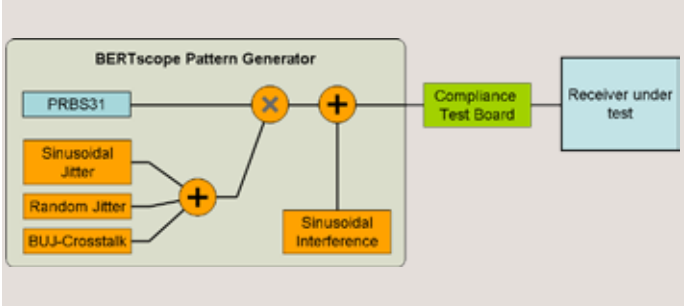


**Figure 14.** Electrical stressed receiver test setup.

To configure the stressed signal, connect the compliance test board between the BERTScope's pattern generator output and error detector input, Figure 14. Generate a PRBS31 test pattern; a long pattern with every permutation of 31 symbols to produce every imaginable bit trajectory.

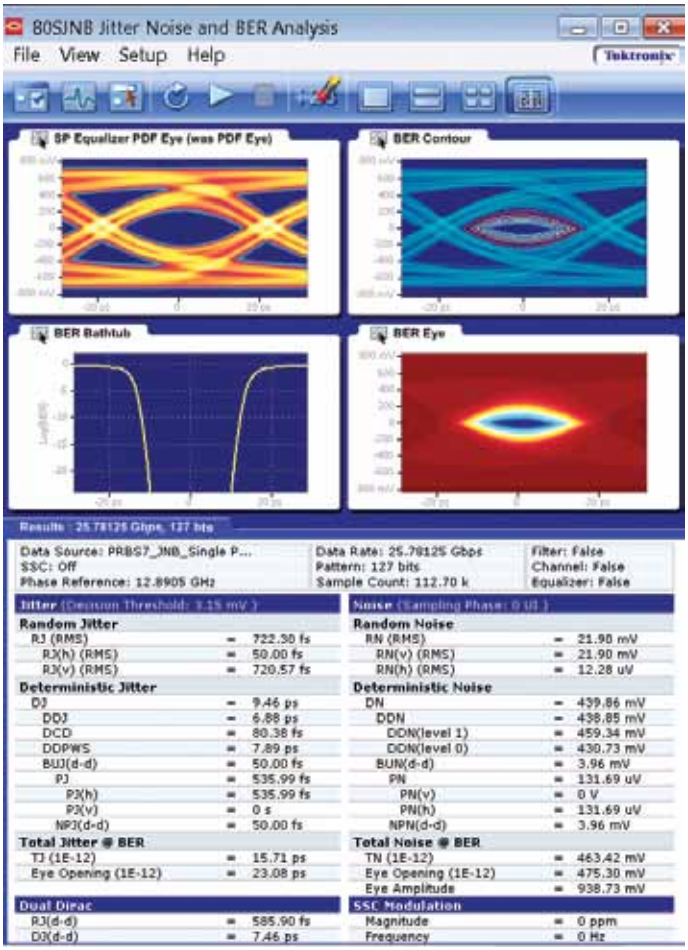


**Figure 15.** A stressed signal.

**Apply DJ**, in addition to that of the compliance test board, by adding a low pass filter and 0.05 UI of SJ at a frequency just above the roll off in Figure 7.

**Apply BUJ-crosstalk** as described in the Appendix – BUJ-crosstalk emulation.

Set the signal amplitude to the specified level, about 600 mV.

**Add sinusoidal interference** to the jittered signal to emulate PCB loss beyond that of the compliance board so that the test signal has the required EH($10^{-15}$), about 240 mV

**Add RJ** until TJ($10^{-15}$) reaches the specified level.

You can see the impact of the stress on the signal in Figure 15.

To perform the test, do whatever you can to assure that the receiver sees the signal you've configured. It's best to connect the receiver to the compliance board with the same cable used to set up the test.

If the receiver is capable of counting its own BER, you're ready to go. If not, connect the receiver output to the BERTScope error detector. If the receiver doesn't provide a clock output, you should use a clock recovery unit to time the error detector. If you don't have a clock recovery unit, you might be able to use the BERTScope data rate clock since the output of the receiver has been retimed.

Apply the stressed signal to the receiver first with low amplitude SJ applied above the roll off frequency, Figure 7. If the receiver operates at or better than the specified BER with its equalization scheme enabled and optimized, continue testing across the SJ frequency-amplitude template in Figure 7 to assure that the receiver can track low-frequency jitter, with all other stresses applied. It's automatic with the BERTScope's Jitter Transfer measurement function.

The receiver is compliant if it operates at or better than the specified BER across the SJ frequency range.

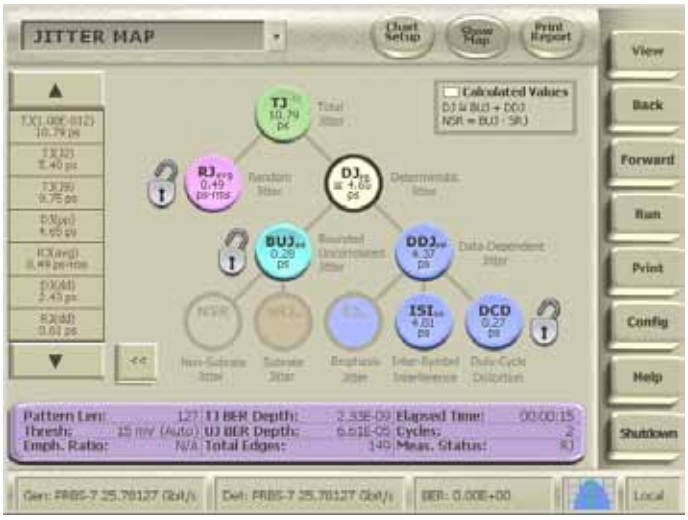


**Figure 16.** Example of jitter decomposition on a BERTScope.

# 4. Diagnostic tests

The difference between compliance and diagnostic tests is complexity. Compliance tests tend to include too many elements for straightforward interpretation. To determine which elements or components of a system might be causing problems, diagnostic tests should be strategically planned to probe specific weaknesses. They should build in complexity, test upon test, to find problems and determine margins.

## 4.1. What to do if the transmitter fails

If the transmitter fails, simplify the test conditions by removing any test compliance boards and analyzing the transmitter output with as direct a connection as possible. Perform jitter and noise analysis. Analyze the breakdown as you apply more complex patterns, introduce increasing lengths of PCB, apply pre-emphasis, and turn on crosstalk aggressors. For each set of conditions, analyze eye diagrams, BER-eye, BER-contours and the jitter and noise breakdown. See Figure 16.

The DSA8300 with 80SJNB software and the BERTScope with the Jitter Map option automatically distinguish different types of jitter which helps isolate problems:

- Non-periodic BUJ → crosstalk isn't being sufficiently shielded.
- DCD → transmitter distortion.
- ISI → trouble with the output path.
- High levels of RJ → problems with transmitter clocking.
- SJ and Periodic Jitter (PJ), sinusoidal and periodic noise → electromagnetic interference from a nearby component, perhaps a switching power supply. Identify the source of interference by studying the jitter frequency spectrum. The clock recovery unit, CR286A, measures the real time jitter spectrum. Do the frequencies of any spectral peaks correspond to harmonics of other components?

## 4.2. What to do if the receiver fails

Investigate the receiver's response to each stress. Use the features of the BERTScope's pattern generator function. Start with a clean pattern and add complexity.

- Apply test patterns with low mark density to check for baseline wander.
- Challenge clock recovery circuits with patterns that have long strings of Consecutive Identical (CID) bits and low transition density. The more structure a pattern has, the more ISI it generates when applied to a compliance board or filter.
- Sweep SJ across the receiver's clock recovery frequency response at different amplitudes. Determine where the clock recovery circuit's ability to track jitter breaks down.
- Challenge the receiver's equalizer by introducing increasing lengths of compliance board. By combining pattern complexity and trace length, you can generate a wide variety of ISI levels and find an equalizer's margin.
- Probe the receiver's ability to tolerate jitter and noise, that is, its setup and hold, by ramping up BUJ-crosstalk and RJ.
- Check the voltage sensitivity by introducing sinusoidal interference.

Find the sensitive aspects of the receiver and then apply different stress combinations. There may be stress combinations that are particularly challenging as well as peculiar combinations where the receiver is quite robust.

## Summary

Signal transmission at 100 Gb/s is not simple. You need high performance test equipment to evaluate the performance of every component and the system as a whole. Between the DSA8300, the BERTScope, and CR286A clock recovery unit, Tektronix provides a complete set of tools for both optical and electrical transmitter and receiver compliance and diagnostic testing.

# Appendix – BUJ-crosstalk emulation

Crosstalk is an important stress for electrical receivers that's easy to emulate by applying PRBS Bounded Uncorrelated Jitter (BUJ). The technique has been employed by HSS standards for the last decade and is easy to implement on a BERTScope. The alternative to emulating crosstalk with BUJ is to purchase at least three more 25+ Gb/s pattern generators.

A PRBS pattern is applied to the voltage-delay of the pattern generator so that it shifts transition timing. This PRBS timing noise causes abrupt shifts in signal timing that is asynchronous with the signal but comes in integer multiples of the bit period, just like the crosstalk required in the specifications.

To calibrate the PRBS BUJ-crosstalk signal for an *N* channel system, connect the pattern generator to a differential aggressor channel and connect the differential victim channel to an oscilloscope. Measure the rms crosstalk voltage noise, $X_{rms}$, on the oscilloscope. Repeat the measurement for the other aggressor channels to get {$X_{rms}$ (1), $X_{rms}$ (2), …, $X_{rms}$ (*N*-1)}. The voltage-to-timing noise equivalent for each aggressor is

$$\text{BUJ-crosstalk for one aggressor} \approx \frac{5\sqrt{2}}{3}\frac{t_{rf}X_{rms}}{V_{Swing}}$$

where $t_{rf}$ is the 20-80% rise/fall time of the clean signal and $V_{Swing}$ is the difference in the average high and low logic voltages. The BUJ-crosstalk equivalent for an *N* channel system is:

$$\text{BUJ-crosstalk for } N\text{-1 aggressors} \approx \frac{5\sqrt{2}}{3}\frac{t_{rf}}{V_{Swing}}\sqrt{X_{rms}(1)^2 + X_{rms}(2)^2 + \cdots + X_{rms}(N-1)^2}$$

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